UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,334	06/26/2003	James D. Welch		2776

7590 10/05/2004

JAMES D. WELCH
10328 PINEHURST AVE.
OMAHA, NE 68124

EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,334	WELCH, JAMES D.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-21 and 23-27* is/are rejected.

7)☒ Claim(s) *1 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's election with traverse of claims 1-4 and 22-24 in the reply filed on 7/6/04 is acknowledged. The traversal is on the ground(s) that, as established in the prosecution of the 6,624,493 Patent, the Examiner has no prior art on which to base a rejection of any semiconductor device whatsoever which is fabricated in compensated semiconductor. This is found persuasive and the Examiner withdraws the restriction requirement.

2. The abstract of the disclosure is objected to because the parentheses in line 2 of the abstract should be deleted. Correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. Claims 1-27 are objected to because of the following informalities: Claim 1, lines 12, 18, 19, claim 2, lines 18, 19, the phrases "at least one junction(s)" and "at least one material(s)" are unclear whether they are being referred to "at least one junction" and "at least one material". Claim 1, line 21, claim 2, lines 21, 29, 36, 42, 50, 56, 75, 83, the phrase "said semiconductor type" has no antecedent basis. Claim 2, lines 27, 34, 40, 48, 54, 73, 81, the phrase "at least one material(s)" is unclear whether it is being referred to "at least one material". Claim 3, lines 36, 37, the phrase "said gate voltage channel induced semiconductor devices" and "said rectifying junctions" have no antecedent basis. Claim 4, line 7, the phrase "said junction non-semiconductor component" has no antecedent basis. Claim 5, lines 7, 11, claim 7, lines 7, 11, claim

11, line 7, claim 12, line 7, claim 17, lines 7, 11, the phrase "said semiconductor" has no antecedent basis. Claim 11, lines 6-7, claims 12, lines 6-7, claim 15, line 19, claim 16, line 19, claim 21, line 18, the phrase "the semiconductor" has no antecedent basis. Appropriate correction is required.

5. Claims 2-21 and 23-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, lines 23-30, it is unclear whether there are two junctions in group (a) and the first junction is ohmic and the second junction forms a rectifying junction; lines 31-43, it is unclear whether there are two junctions in group (b) and the first junction forms a rectifying junction and the second junction forms a rectifying junction; lines 44-58, it is unclear whether there are four junctions in group (c) and the first junction is ohmic, the second junction forms a rectifying junction, the third junction forms a rectifying junction and the fourth junction is ohmic; lines 59-63, it is unclear whether there are four junctions in group (d) and the first junction is ohmic, the second junction forms a rectifying junction, the third junction forms a rectifying junction and the fourth junction is ohmic; lines 64-66, it is unclear whether there are two junctions in group (e) and the first junction forms a rectifying junction and the second junction forms a rectifying junction; lines 67-69, it is unclear whether there are two junctions in group (f) and the first junction is ohmic and the second junction forms a rectifying junction; lines 70-84, it is unclear whether there are four junctions in group (g) and the first junction forms a

rectifying junction, the second junction is ohmic, the third junction is ohmic and the fourth junction forms a rectifying junction.

Claim 3, lines 3-5, it is unclear whether each of the inverting and non-inverting devices comprising two oppositely facing electrically interconnected rectifying diodes in a semiconductor region of a substrate; lines 18-19, the phrase "said inverting and non-inverting single device equivalents to dual device seriesed N and P-Channel MOSFETS CMOS systems" is unclear whether it is being referred to "each of said inverting and non-inverting single devices equivalents to dual device seriesed N and P-Channel MOSFETS CMOS systems"; line 39, the word "it" is unclear whether it is being referred to the semiconductor region.

Claim 4, line 8, the word "material(s)" is unclear whether there is one material or more than one material.

Claim 5, line 60, claim 7, line 57, the word "it" is unclear whether it is being referred to the semiconductor channel region.

Claim 15, lines 7-19, claim 16, lines 7-20, it is unclear which process steps are used to form the source junction and which process steps are used to form the drain junction.

Claim 17, line 43, the word "semiconductor" is unclear whether it is being referred to the semiconductor epi-layer or substrate; line 43, the word "it" is unclear whether it is being referred to the semiconductor epi-layer or substrate.

Claim 25, line 1, the phrase "A semiconductor system" is unclear because there is no semiconductor system in claim 5.

Claim 26, line 1, the phrase "A semiconductor system" is unclear because there is no semiconductor system in claim 7.

Claim 27, line 1, the phrase "A semiconductor system" is unclear because there is no semiconductor system in claim 17.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 4 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Nowak (U.S. Patent no. 5,250,834 in the IDS filed on 6/26/03).

In regards to claim 4, Nowak shows all the elements of the claimed invention in figs. 1 and 2. It is a semiconductor device formed in a semiconductor region [120] characterized as single crystal (col. 4, lines 60-67) thereto, in which are essentially homogeneously simultaneously present both N and P-type metallurgical dopants (col. 2, line 46 to col. 3, line 16) (region [120] contains both n-type and p-type dopants), said semiconductor device comprising at least one rectifying junction (the refractory metal silicide formed on the region [120] of the interconnect region [132]) (col. 4, line 7 to col. 5, line 42) which is formed from non-semiconductor (refractory metal silicide) and semiconductor (silicon) components, wherein said non-semiconductor component is comprised of material which, in use, form a rectifying junction with both N and P-type metallurgically induced semiconductor (p-type region [106] and n-type region [120]).

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 5-8, 10-21 and 25-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,624,493 (Welch). Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 5, 7 and 17 of the present application and claims 1, 6 and 12 of the patent disclose an inverting gate voltage channel induced semiconductor device being formed in a semiconductor epi-layer or substrate characterized by a selection from the group consisting of: said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and said semiconductor contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels.

Claims 5, 7 and 17 differs from claims 1, 6 and 12 of the patent by not showing the presence of at least partially compensated semiconductor which comprises both N and P-type carriers enables easy provision of N and P-type channel region forming carriers via gate voltage application effected field effect means.

Since claims 5, 7 and 17 of the present application and claims 1, 6 and 12 of the patent show the semiconductor is formed in a semiconductor contains homogeneously distributed N and P-type metallurgical dopants, it would have obvious for claims 5, 7 and 17 of the present application to have the at least partially compensated semiconductor which comprises both N and P-type carriers enables easy provision of N and P-type channel region forming carriers via gate voltage application effected field effect means because the semiconductor epi-layer always contains constant amount of dopants throughout the entire epi-layer. Since the top surface of the epi-layer comprises both n and p-type dopants, the semiconductor device of claims 5, 7 and 17 would allow easy provision of N and P-type channel region forming carriers via gate voltage application effected field effect means.

The claimed subject matters of claims 6, 11, 13 and 15 of the present application are identical to claims 2, 3, 4 and 5 of the patent, respectively.

The claimed subject matters of claims 8, 10, 12, 14 and 16 of the present application are identical to claims 7, 8, 9, 10 and 11 of the patent, respectively.

The claimed subject matters of claims 18, 19, 20 and 21 of the present application are identical to claims 13, 14, 15 and 16 of the patent, respectively.

Claims 25-27 differ from the claims in the patent by not showing the semiconductor epi-layer or substrate is single crystal.

It would have been obvious for the semiconductor epi-layer or substrate is single crystal because it has high electron mobility and it is a conventional semiconductor material.

10. Claim 1 is would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

11. Claims 2 and 3 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

12. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is a semiconductor region of a substrate characterized by at least one selection from the group consisting of: said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially equal doping levels; and said semiconductor region contains both N and P-type metallurgical dopants essentially homogeneously distributed therein at substantially different doping levels. The second major difference in the claims not found in the prior art of record is a semiconductor channel region and, when formed, adjacent drain junction which is not forward conducting, is characterized by at least one selection from the group consisting of: a. being functionally comprised of two regions across which voltage can drop, namely an onset of pinch-off region and a channel region; b. being functionally comprised of three regions across which voltage can drop, namely an onset of pinch-off region, a portion of the channel region which is populated with some gate voltage field induced carriers, and a formed reverse biased rectifying junction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl

September 29, 2004

Steven Loke
Primary Examiner